11.3 Gbps Differential VCSEL Driver With Output Waveform Shaping

FEATURES

- **Up to 11.3 Gbps Operation**
- **2-Wire Digital Interface**
- **Digitally Selectable Modulation Current up to 24 mApp Differential**
- **Digitally Selectable Bias Current up to 20 mA**
- **Automatic Power Control (APC) Loop**
- **Supports Transceiver Management System (TMS)**
- **Programmable Input Equalizer**
- **Output Waveform Control**
- **Includes Laser Safety Features**
- **Analog Temperature Sensor Output**
- **Selectable Monitor Photodiode Current Range**
- **Output Polarity Select**
- **Single 3.3V Supply**
- **Operating Temperature –40°C to 85°C**
- **Surface Mount Small Footprint 4mm × 4mm 20 Pin RoHS compliant QFN Package**

APPLICATIONS

- **10 Gigabit Ethernet Optical Transmitters**
- **8x and 10x Fibre Channel Optical Transmitters**
- **SONET OC-192/SDH STM-64 Optical Transmitters**
- **SFP+ and XFP Transceiver Modules**
- **XENPAK, XPAK, X2 and 300-pin MSA Transponder Modules**

DESCRIPTION

The ONET8501V is a high-speed, 3.3V laser driver designed to directly modulate VCSELs at data rates from 2 Gbps up to 11.3 Gbps.

The device provides a two-wire serial interface which allows digital control of the modulation and bias currents, eliminating the need for external components. Output waveform control, in the form of cross point control and independent over- and undershoot capability on the rising and falling edges is also available to improve VCSEL edge speeds and the optical eye diagram. An optional input equalizer can be used for equalization of up to 300mm (12 inch) of microstrip or stripline transmission line on FR4 printed circuit boards.

The ONET8501V includes an integrated automatic power control (APC) loop as well as circuitry to support laser safety and transceiver management systems. The VCSEL driver is characterized for operation from –40°C to 85°C ambient temperatures and is available in a small footprint 4mm × 4mm 20 pin RoHS compliant QFN package.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

BLOCK DIAGRAM

A simplified block diagram of the ONET8501V is shown in Figure 1.

The VCSEL driver consists of an equalizer, a limiter, a waveform shaping block with over- and undershoot control, an output driver, power-on reset circuitry, a 2-wire serial interface including a control logic block, a modulation current generator and a bias current generator with automatic power control loop, and an analog reference block.

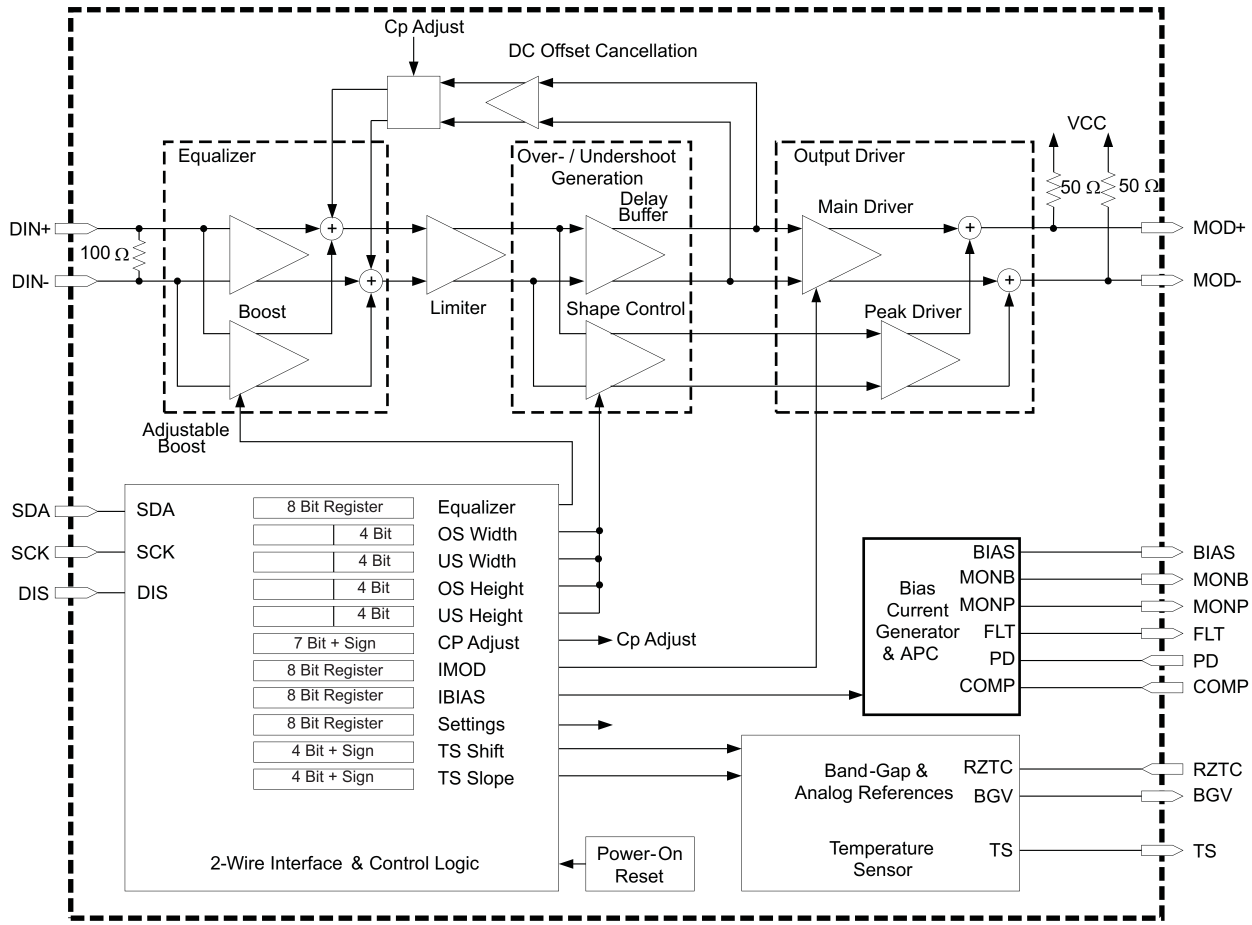
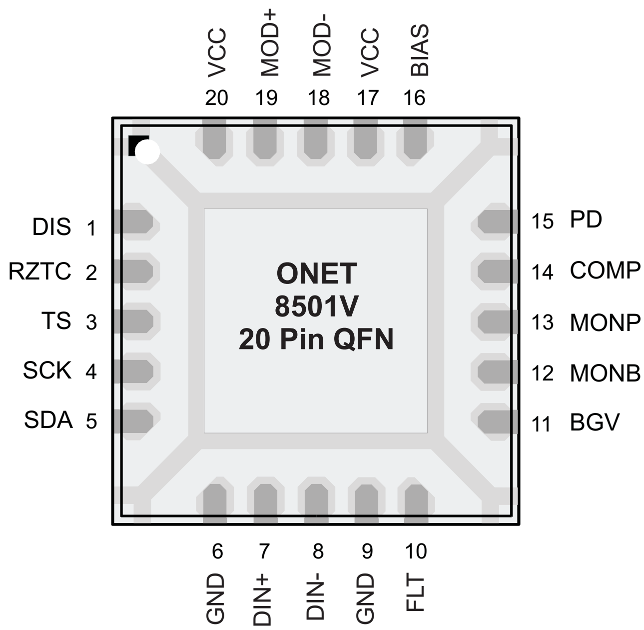


Figure 1. Simplified Block Diagram of the ONET8501V

PACKAGE

The ONET8501V is packaged in a small footprint 4mm × 4mm 20 pin RoHS compliant QFN package with a lead pitch of 0,5 mm. The pin out is shown below.

20 PIN QFN PACKAGE
4 mm × 4 mm (TOP VIEW)



TERMINAL FUNCTIONS

TERMINAL			
PIN NO.	**NAME**	**TYPE**	**DESCRIPTION**
1	DIS	Digital-in	Disables bias, modulation and peaking currents when set to high state. Toggle to reset a fault condition. Recommend shorting pin to GND if disable feature is not used.
2	RZTC	Analog	Connect external zero TC 28.7kΩ resistor to ground (GND). Used to generate a defined zero TC reference current for internal DACs.
3	TS	Analog-out	Temperature sensor output.
4	SCK	Digital -in	2-wire interface serial clock. Includes a pull-up resistor to VCC.
5	SDA	Digital -in	2-wire interface serial data input. Includes a pull-up resistor to VCC.
6, 9, EP	GND	Supply	Circuit ground. Exposed die pad (EP) must be grounded.
7	DIN+	Analog-in	Non-inverted data input. On-chip differentially 100Ω terminated to DIN–. Must be AC coupled.
8	DIN–	Analog-in	Inverted data input. On-chip differentially 100Ω terminated to DIN+. Must be AC coupled.
10	FLT	Digital-out	Fault detection flag. LVCMOS output with source and sink capability.
11	BGV	Anolog-out	Buffered bandgap voltage with 1.16V output. This is a replica of the bandgap voltage at RZTC. For best matching, use the same 28.7kΩ resistor to GND as used at RZTC.
12	MONB	Analog-out	Bias current monitor. Sources a 3.5% replica of the bias current. Connect an external resistor to ground (GND). If the voltage at this pin exceeds 1.16V a fault is triggered. Typically choose a resistor to give MONB voltage of 0.8V at the maximum desired bias current.
13	MONP		Photodiode current monitor. Sources a 27% replica of the photodiode current when PDR = 10, a 54% replica when PDR = 01, and a 270% replica when PDR=00. Connect an external resistor (5kΩ typical) to ground (GND).
14	COMP	Analog	Compensation pin used to control the bandwidth of the APC loop. Connect a 0.01µF capacitor to ground.
15	PD		Photodiode input. Pin can source or sink current dependent on register setting.
16	BIAS		Sinks average bias current for VCSEL in both APC and open loop modes. Connect to laser cathode through an inductor. BLM15HG102SN1D recommended.
17, 20	VCC	Supply	3.3V ± 10% supply voltage

TERMINAL FUNCTIONS (continued)

TERMINAL			
PIN NO.	NAME	TYPE	DESCRIPTION
18	MOD–	CML-out (current)	Inverted modulation current output. On-chip 50Ω back-terminated to VCC. I_{MOD} flows into this pin when input data is low.
19	MOD+	CML-out (current)	Non-inverted modulation current output. On-chip 50Ω back-terminated to VCC. I_{MOD} flows into this pin when input data is high.

ABSOLUTE MAXIMUM RATINGS[1]

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
V_{CC}	Supply voltage[2]	–0.3 to 4	V
V_{DIS}, V_{RZTC}, V_{TS}, V_{SCK}, V_{SDA}, V_{FLT}, V_{BGV}, V_{MONB}, V_{MONP}, V_{CAPC}, V_{PD}, V_{BIAS} V_{DIN+}, V_{DIN-}, V_{MOD+}, V_{MOD-}	Voltage at DIS, RZTC, TS, SCK, SDA, FLT, BGV, MONB, MONP, CAPC, PD, BIAS, DIN+, DIN–, MOD+, MOD–[2]	–0.3 to 4	V
I_{DIN-}, I_{DIN+}	Maximum current at input pins	25	mA
I_{MOD+}, I_{MOD-}	Maximum current at output pins	30	mA
ESD	ESD rating at all pins	2	kV (HBM)
$T_{J,max}$	Maximum junction temperature	125	°C
T_{STG}	Storage temperature range	–65 to 150	°C
T_A	Characterized free-air operating temperature range	–40 to 85	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability
(2) All voltage values are with respect to network ground terminal

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

			MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		2.95	3.3	3.6	V
V_{IH}	Digital input high voltage	DIS, SCK, SDA	2			V
V_{IL}	Digital input low voltage	DIS, SCK, SDA			0.8	V
	Bias output headroom voltage	V_{BIAS} – GND	300			mV
	Photodiode current range	High step size mode, min. step size = 5 µA		25		µA
		High step size mode, max. step size = 5 µA		1280		
		Medium step size mode, min. step size = 2.5 µA		12.5		
		Medium step size mode, max. step size = 2.5 µA		640		
		Low step size mode, min. step size = 0.5 µA		2.5		
		Low step size mode, max. step size = 0.5 µA		128		
R_{RZTC}	Zero TC resistor value[1]	1.16 V bandgap bias across resistor, E96, 1% accuracy	28.4	28.7	29	kΩ
v_{IN}	Differential input voltage swing		100		1200	mV_{pp}
t_{R-IN}	Input rise time	20%–80%		30	55	ps
t_{F-IN}	Input fall time	20%–80%		30	55	ps
T_A	Operating free-air temperature		–40		85	°C

(1) Changing the value will alter the DAC ranges.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions, all values are for open-loop operation, I_{MODC} = 12 mA, I_{BIASC} = 6 mA, and R_{RZTC} = 28.7 kΩ, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		2.95	3.3	3.6	V
I_{VCC}	Supply current	I_{MODC} = 12 mA, I_{BIASC} = 6 mA, including I_{MODC}, No waveform shaping, EQENA = 0		50	70	mA
		I_{MODC} = 12 mA, I_{BIASC} = 6 mA, including I_{MODC}, No waveform shaping, EQENA = 1		55	75	
		I_{MODC} = 12 mA, I_{BIASC} = 6 mA, including I_{MODC}, Single sided max output waveform shaping at MOD+ or MOD–, EQENA = 1		75	90	
		I_{MODC} = 12 mA, I_{BIASC} = 6 mA, including I_{MODC}, Double sided max output waveform shaping at MOD+ or MOD–, EQENA = 1		82	100	
		Disabled (DIS=HIGH) or ENA=LOW, EQENA = 0		24		
R_{IN}	Data input resistance	Differential between DIN+ / DIN–	80	100	120	Ω
R_{OUT}	Data output resistance	Single-ended to VCC	40	50	60	Ω
	Digital input current	SCK, SDA, pull up to VCC(1)	–10		10	µA
	Digital input current	DIS, pull down to GND(1)	–10		10	µA
V_{OH}	Digital output high voltage	FLT, pull-up to V_{CC}, I_{SOURCE} = 1000 µA(2)	2.4			V
V_{OL}	Digital output low voltage	FLT, pull-up to V_{CC}, I_{SINK} = 1000 µA(2)			0.4	V
$I_{BIAS-DIS}$	Bias current during disable				100	µA
$I_{BIAS-MIN}$	Minimum bias current	See (3)			200	µA
$I_{BIAS-MAX}$	Maximum bias current	DAC set to maximum, open and closed loop	17	20		mA
V_{PD}	Photodiode reverse bias voltage	APC active, I_{PD} = max	1.3	2.3		V
	Photodiode fault current level	Percent of target I_{PD} (1)		150%		
V_{TS}	Temperature sensor voltage range	–40°C to 120°C junction temperature. With Mid scale calibration(1)	0.5		2.5	V
	Temperature sensor accuracy	With mid scale calibration(1)		±4		°C
I_{TS}	Temperature sensor drive current	Source or sink (1)		100		µA
	Photodiode current monitor ratio	I_{MONP} / I_{PD} with control bit PDR = 10	20%	27%	32%	
		I_{MONP} / I_{PD} with control bit PDR = 01	40%	54%	65%	
		I_{MONP} / I_{PD} with control bit PDR = 00	200%	270%	350%	
	Bias current monitor ratio	I_{MONB} / I_{BIAS} (nominal 1/30 = 3.3%) 1.2 kΩ sense resistor.	2.9%	3.5%	4.2%	
V_{CC-RST}	VCC reset threshold voltage	V_{CC} voltage level which triggers power-on reset	2.4	2.5	2.8	V
$V_{CC-RSTHYS}$	VCC reset threshold voltage hysteresis			100		mV
$V_{MONB-FLT}$	Fault voltage at MONB	Fault occurs if voltage at MONB exceeds value	1.1	1.16	1.2	V

(1) Specified by simulation over process, supply and temperature variation
(2) External pull up resistor according to timing requirements
(3) The bias current can be set below the specified minimum according to the corresponding register setting, however in closed loop operation settings below the specified value may trigger a fault.

AC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions with 50Ω output load, open loop operation, I_{MODC} = 12 mA, I_{BIAS} = 6 mA, and R_{RZTC} = 28.7 kΩ, unless otherwise noted. Typical operating condition is at V_{CC} = 3.3V and T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SDD11	Differential input return gain	0.01 GHz < f < 3.9 GHz		–16		dB
		3.9 GHz < f < 11.1 GHz		(1)		
		11.1 GHz < f < 20 GHz		–3		
SCD11	Differential to common mode conversion gain	f < 8.25 GHz		–35		dB
		8.25 GHz < f < 20 GHz		–28		
t_{R-OUT}	Output rise time	20% – 80%, t_{R-IN} < 40 ps, 100 Ω differential load, no waveform shaping, EQENA = 0, 100 mVpp differential input voltage		24	30	ps
t_{F-OUT}	Output fall time	20% – 80%, t_{F-IN} < 40 ps, 100 Ω differential load, no waveform shaping, EQENA = 0, 100 mVpp differential input voltage		24	30	
$I_{MOD-MAX}$	Maximum modulation current	Output stage tail current	16	24		mA
$I_{MOD-STEP}$	Modulation current step size full			100		μA
	Modulation current step size half	Modulation current smaller than 6 mA		50		
DJ	Deterministic output jitter	EQENA = 0, K28.5 pattern at 11.3 Gbps, no waveform shaping, 100 mVpp, 600 mVpp, 1200 mVpp differential input voltage		3.5	9	ps_{p-p}
		EQENA = 1, K28.5 pattern at 11.3 Gbps, maximum equalization with 12” transmission line at the input, no waveform shaping, 200 mVpp, 600 mVpp, 1200 mVpp differential input voltage		8.5	15	
	Maximum output peaking width	Maximum peaking height (2)		120		ps
	Minimum output peaking width			30		
	Maximum output peaking height	Referred to output stage tail current, high range		10		mA
		Referred to output stage tail current, low range		5		
	Output peaking height step size	Referred to output stage tail current, high range		0.66		mA
		Referred to output stage tail current, low range		0.33		
	Cross point range	600 mVpp differential input		30–70%		
RJ	Random output jitter	50Ω load, EQENA = 0, 100 mVpp differential input voltage		0.4	0.6	ps_{RMS}
τ_{APC}	APC time constant	C_{APC} 0.01 μF, I_{PD} = 100 μA, PD coupling ratio CR = 40 (2)		200		μs
t_{OFF}	Transmitter disable time	Rising edge of DIS to $I_{BIAS} \le 0.1\times I_{BIAS-NOMINAL}$ (2)		1	5	μs
t_{ON}	Disable negate time	Falling edge of DIS to $I_{BIAS} \ge 0.9 \times I_{BIAS-NOMINAL}$ (2)			1	ms
t_{INIT1}	Power-on to initialize	Power-on to registers ready to be loaded		0.2	1	ms
t_{INIT2}	Initialize to transmit	Register load STOP command to part ready to transmit valid data (2)			2	ms
t_{RESET}	DIS pulse width	Time DIS must held high to reset part (2)	100			ns
t_{FAULT}	Fault assert time	Time from fault condition to FLT high (2)			50	μs

(1) Differential Return Gain given by SDD11 = –14 + 13.33 $\log_{10}$(f/5.5), f in GHz
(2) Assured by simulation over process, supply and temperature variation

DETAILED DESCRIPTION

EQUALIZER

The data signal can be applied to an input equalizer by means of the input signal pins DIN+/DIN–, which provide on-chip differential 100Ω line-termination. The equalizer is enabled by setting the EQENA = 1 (bit 1 of register 0). Equalization of up to 300mm (12”) of microstrip or stripline transmission line on FR4 printed circuit boards can be achieved. The amount of equalization is digitally controlled by the two-wire interface and control logic block and depends on the register settings EQADJ[0..7] (register 3). The equalizer can also be turned off and bypassed by setting EQENA = 0. For details about the equalizer settings, see Table 16.

LIMITER

By limiting the output signal of the equalizer to a fixed value, the limiter removes any overshoot after the input equalization and provides the input signal for the output signal waveform shaping.

OUTPUT SIGNAL WAVEFORM SHAPING

The output signal waveform shaping provides two paths for the data signal. The delay buffer ensures that both paths have the same transit time. The over- and undershoot peaking width and height are controlled through the two wire interface and the peak driver linearly amplifies the signal. The resultant waveform shaped signal is then added to the output of the main driver. The overshoot width is controlled by register 5 settings OSW[0..3] and the overshoot height is controlled by register 6 settings OSH[0..3]. The undershoot width is controlled by register 7 settings USW[0..3] and the undershoot height is controlled by register 8 settings OSH[0..3].

The peaking current is disabled by setting both over- and undershoot height registers to zero. The peaking current is also disabled when the DIS pin is set to a high level or during a fault condition if the fault detection enable register flag FLTEN is set (bit 3 of register 0).

HIGH-SPEED OUTPUT DRIVER

The modulation current is sunk from the common emitter node of the output driver differential pair by means of a modulation current generator, which is digitally controlled by the 2-wire serial interface.

The collector nodes of the output stages are connected to the output pins MOD+/ MOD–, which include on-chip 2 × 50Ω back-termination to VCC. The 50Ω back-termination together with an optional off chip series resistor helps to sufficiently suppress signal distortion caused by double reflections for VCSEL diodes with impedances from 50Ω through 110Ω. The polarity of the output can be selected with the output polarity switch POL (bit 4 of register 9).

MODULATION CURRENT GENERATOR

The modulation current generator provides the current for the current modulator described above. The circuit is digitally controlled by the 2-wire interface block.

An 8-bit wide control bus, MODC[0..7] (register 1), is used to set the desired modulation current. Furthermore, four modulation current ranges can be selected by means of MODRNG1 (bit 1 of register 13) and MODRNG0 (bit 0 of register 13).

The modulation current can be disabled by setting the DIS input pin to a high level. The modulation current is also disabled in a fault condition if the fault detection enable register flag FLTEN is set (bit 3 of register 0).

DC OFFSET CANCELLATION AND CROSS POINT CONTROL

The ONET8501V has DC offset cancellation to compensate for internal offset voltages. The offset cancellation can be disabled by setting OCDIS = 1 (bit 2 of register 9). Disabling the offset cancellation enables the output crossing point to be adjusted from 35% to 65% of the output eye diagram. The crossing point can be moved toward the one level be setting CPSGN = 1 (bit 7 of register 4) and it can be moved toward the zero level by setting CPSGN = 0. The percentage of shift depends upon the register settings CPADJ[0..6] (register 4).

BIAS CURRENT GENERATION AND APC LOOP

The bias current generation and APC loop are controlled by means of the 2-wire interface. In open loop operation, selected by setting OLENA = 1 (bit 4 of register 0) the bias current is set directly by the 8-bit wide control word BIASC[0..7] (register 2). In automatic power control mode, selected by setting OLENA = 0, the bias current depends on the register settings BIASC[0..7] and the coupling ratio (CR) between the VCSEL bias current and the photodiode current. CR = $I_{BIAS\text{-}VCSEL}$/ I_{PD}.

Three photodiode current ranges can be selected by means of the PDRNG[1..0] bits (register 0). The photodiode range should be chosen to keep the laser bias control DAC, BIASC[0..7], close to the center of its range. This keeps the laser bias current set point resolution high.

For details regarding the bias current setting in open- as well as in closed-loop mode, see Table 16.

In closed-loop mode, the photodiode polarity bit, PDPOL (bit 0 of register 0), must be set for common-anode or common-cathode configuration to ensure proper operation.

ANALOG REFERENCE AND TEMPERATURE SENSOR

The ONET8501V VCSEL driver is supplied by a single 3.3V10% supply voltage connected to the VCC pins. This voltage is referred to ground (GND).

On-chip bandgap voltage circuitry generates a reference voltage, independent of the supply voltage, from which all other internally required voltages and bias currents are derived.

An external zero temperature coefficient resistor must be connected from the RZTC pin of the device to ground (GND). This resistor is used to generate a precise, zero-TC current which is required as a reference current for the on-chip DACs.

In order to minimize the module component count, the ONET8501V provides an on-chip temperature sensor. The output voltage of the temperature sensor is available at the TS pin. Due to the die temperature of the 8501V and for high accuracy applications, the use of an external temperature sensor may be required. However, in order to improve the part-to-part accuracy of the sensor, the offset voltage and temperature slope can be adjusted through the 2-wire interface. The offset voltage can be adjusted by means of the TSSH[0..3] bits (register 10) and the direction of the offset can be set by the sign bit TSHSGN (bit 4 of register 10). The temperature slope can be adjusted by means of the TSSL[0..3] bits (register 11) and the sign bit TSLSGN (bit 4 of register 11).

The temperature sensor can be disabled by setting TSDIS = 1 (bit 1 of register 9).

POWER-ON RESET

The ONET8501V has power on reset circuitry which ensures that all registers are reset to zero during startup. After the power-on to initialize time (t_{INIT1}), the internal registers are ready to be loaded. The part is ready to transmit data after the initialize to transmit time (t_{INIT2}), assuming that the chip enable bit ENA is set to 1 and the disable pin DIS is low.

The ONET8501V can be disabled using either the ENA control register bit or the disable pin DIS. In both cases the internal registers are not reset. After the disable pin DIS is set low and/or the enable bit ENA is set back to 1, the part returns to its prior output settings.

2-WIRE INTERFACE AND CONTROL LOGIC

The ONET8501V uses a 2-wire serial interface for digital control. The two circuit inputs, SDA and SCK, are driven, respectively, by the serial data and serial clock from a microcontroller, for example. Both inputs include 500kΩ pull-up resistors to VCC. For driving these inputs, an open drain output is recommended.

The 2-wire interface allows write access to the internal memory map to modify control registers and read access to read out the control signals. The ONET8501V is a slave device only which means that it cannot initiate a transmission itself; it always relies on the availability of the SCK signal for the duration of the transmission. The master device provides the clock signal as well as the START and STOP commands. The protocol for a data transmission is as follows:

1. START command
2. 7 bit slave address (0001000) followed by an eighth bit which is the data direction bit (R/W). A zero indicates a WRITE and a 1 indicates a READ.
3. 8 bit register address
4. 8 bit register data word
5. STOP command

Regarding timing, the ONET8501V is I^2C compatible. The typical timing is shown in Figure 2 and a complete data transfer is shown in Figure 3. Parameters for Figure 2 are defined in Table 1.

Bus Idle: Both SDA and SCK lines remain HIGH

Start Data Transfer: A change in the state of the SDA line, from HIGH to LOW, while the SCK line is HIGH, defines a START condition (S). Each data transfer is initiated with a START condition.

Stop Data Transfer: A change in the state of the SDA line from LOW to HIGH while the SCK line is HIGH defines a STOP condition (P). Each data transfer is terminated with a STOP condition; however, if the master still wishes to communicate on the bus, it can generate a repeated START condition and address another slave without first generating a STOP condition.

Data Transfer: Only one data byte can be transferred between a START and a STOP condition. The receiver acknowledges the transfer of data.

Acknowledge: Each receiving device, when addressed, is obliged to generate an acknowledge bit. The transmitter releases the SDA line and a device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge clock pulse. Setup and hold times must be taken into account. When a slave-receiver doesn't acknowledge the slave address, the data line must be left HIGH by the slave. The master can then generate a STOP condition to abort the transfer. If the slave-receiver does acknowledge the slave address but some time later in the transfer cannot receive any more data bytes, the master must abort the transfer. This is indicated by the slave generating the not acknowledge on the first byte to follow. The slave leaves the data line HIGH and the master generates the STOP condition.

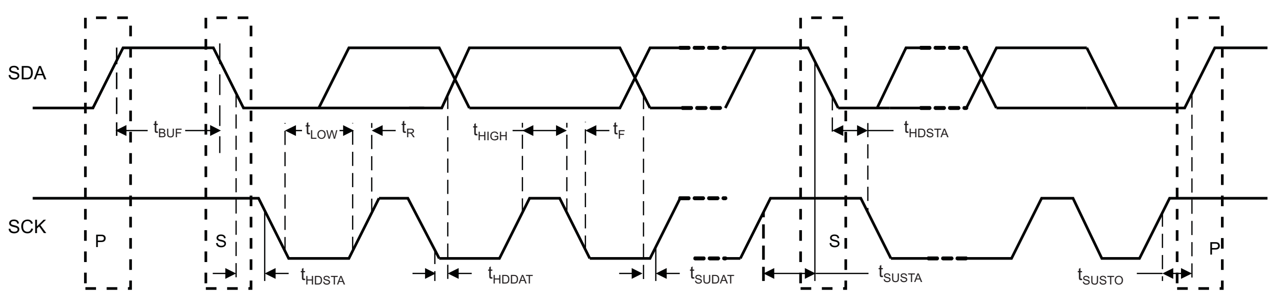


Figure 2. I^2C Timing Diagram

Table 1. Timing Diagram Definitions

PARAMETER	SYMBOL	MIN	MAX	UNIT
SCK clock frequency	f_{SCK}		400	kHz
Bus free time between START and STOP conditions	t_{BUF}	1.3		μs
Hold time after repeated START condition. After this period, the first clock pulse is generated	t_{HDSTA}	0.6		μs
Low period of the SCK clock	t_{LOW}	1.3		μs
High period of the SCK clock	t_{HIGH}	0.6		μs
Setup time for a repeated START condition	t_{SUSTA}	0.6		μs
Data HOLD time	t_{HDDAT}	0		μs
Data setup time	t_{SUDAT}	100		ns
Rise time of both SDA and SCK signals	t_R		300	ns
Fall time of both SDA and SCK signals	t_F		300	ns
Setup time for STOP condition	t_{SUSTO}	0.6		μs

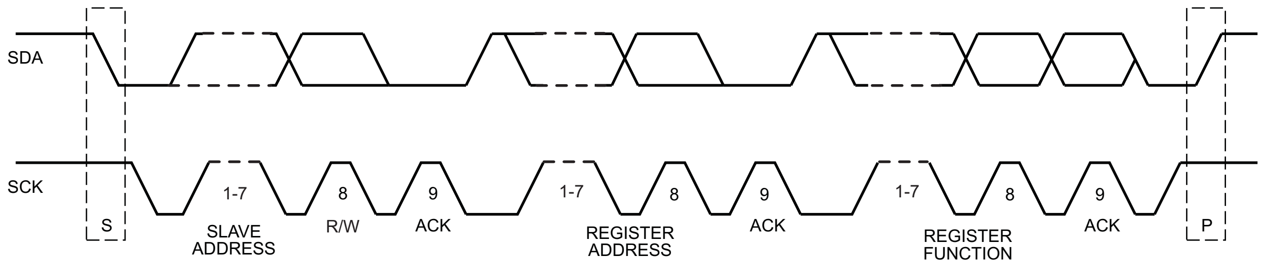


Figure 3. Data Transfer

REGISTER MAPPING

The register mapping for register addresses 0 (0x00) through 13 (0x0D) are shown in Table 2 through Table 15. Table 16 describes the circuit functionality based on the register settings.

Table 2. Register 0 (0x00) Mapping – Control Settings

Register Address 0 (0x00)							
bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
ENA	PDRNG1	PDRNG0	OLENA	FLTEN	PKRNG	EQENA	PDPOL

Table 3. Register 1 (0x01) Mapping – Modulation Current

Register Address 1 (0x01)							
bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
MODC7	MODC6	MODC5	MODC4	MODC3	MODC2	MODC1	MODC0

Table 4. Register 2 (0x02) Mapping – Bias Current

Register Address 2 (0x02)							
bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
BIASC7	BIASC6	BIASC5	BIASC4	BIASC3	BIASC2	BIASC1	BIASC0

Table 5. Register 3 (0x03) Mapping – Equalizer Adjust

Register Address 3 (0x03)							
bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
EQADJ7	EQADJ6	EQADJ5	EQADJ4	EQADJ3	EQADJ2	EQADJ1	EQADJ0

Table 6. Register 4 (0x04) Mapping – Cross Point Adjust

Register Address 4 (0x04)							
bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
CPSGN	CPADJ6	CPADJ5	CPADJ4	CPADJ3	CPADJ2	CPADJ1	CPADJ0

Table 7. Register 5 (0x05) Mapping – Overshoot Width

Register Address 5 (0x05)							
bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
—	—	—	—	OSW3	OSW2	OSW1	OSW0

Table 8. Register 6 (0x06) Mapping – Overshoot Height

Register Address 6 (0x06)							
bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
—	—	—	—	OSH3	OSH2	OSH1	OSH0

Table 9. Register 7 (0x07) Mapping – Undershoot Width

Register Address 7 (0x07)							
bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
—	—	—	—	USW3	USW2	USW1	USW0

Table 10. Register 8 (0x08) Mapping – Undershoot Height

Register Address 8 (0x08)							
bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
—	—	—	—	USH3	USH2	USH1	USH0

Table 11. Register 9 (0x09) Mapping – Control Settings

Register Address 9 (0x09)							
bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
—	—	—	POL	OCSRC	OCDIS	TSDIS	SPDIS

Table 12. Register 10 (0x0A) Mapping – Temperature Sensor Shift

Register Address 10 (0x0A)							
bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
—	—	—	TSHSGN	TSSH3	TSSH2	TSSH1	TSSH0

Table 13. Register 11 (0x0B) Mapping – Temperature Sensor Slope

Register Address 11 (0x0B)							
bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
—	—	—	TSLSGN	TSSL3	TSSL2	TSSL1	TSSL0

Table 14. Register 12 (0x0C) Mapping – Cross Point Range

Register Address 12 (0x0C)							
bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
—	—	—	—	—	—	CPRNG1	CPRNG0

Table 15. Register 13 (0x0D) Mapping – Modulation Range

Register Address 13 (0x0D)							
bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
—	—	—	—	—	—	MODRNG1	MODRNG0

Table 16. Register Functionality

SYMBOL	REGISTER	FUNCTION
ENA	Enable bit 7	**Enable chip bit:** 1 = chip enabled. Can be toggled low to reset a fault condition 0 = chip disabled
PDRNG1 PDRNG0	Photodiode current range bit 6 Photodiode current range bit 5	**Photodiode current range bits:** With Coupling Ratio CR between VCSEL bias current and photodiode current = 30 1X = 25µA – 1280µA / 5µA resolution 01 = 12.5µA – 640µA / 2.5µA resolution 00 = 2.5µA – 128µA / 0.5µA resolution
OLENA	Open loop enable bit 4	**Open loop enable bit:** 1 = open loop bias current control, 0 = closed loop bias current control
FLTEN	Fault detection enable bit 3	**Fault detection enable bit:** 1 = fault detection on 0 = fault detection off
PKRNG	Peaking tail current range bit 2	**Laser peaking tail current range (over- and undershoot):** 1 = 0mA – 12mA 0 = 0mA – 6mA
EQENA	Equalizer Enable bit 1	**Equalizer enable bit** 1 = equalizer enabled 0 = equalizer disabled
PDPOL	Photodiode polarity bit 0	**Photodiode polarity bit:** 1 = photodiode cathode connected to V_{CC} 0 = photodiode anode connected to GND
MODC7	Modulation current bit 7 (MSB)	**Modulation current setting:** MODRNG = 00 (see below); Modulation current: 24 mA / 94 µA steps MODRNG = 01 (see below): Modulation current: 20 mA / 78 µA steps MODRNG = 10 (see below); Modulation current: 15.8 mA / 62 µA steps MODRNG = 11 (see below); Modulation current: 12 mA / 47 µA steps
MODC6	Modulation current bit 6	
MODC5	Modulation current bit 5	
MODC4	Modulation current bit 4	
MODC3	Modulation current bit 3	
MODC2	Modulation current bit 2	
MODC1	Modulation current bit 1	
MODC0	Modulation current bit 0 (LSB)	
BIASC7	Bias current bit 7 (MSB)	**Closed loop (APC):** Coupling ratio CR = $I_{BIAS-VCSEL}$ / I_{PD}, BIASC = 0 .. 255, $I_{BIAS-VCSEL}$ ≤ 20mA: PDRNG = 00 (see above); $I_{BIAS-VCSEL}$ = 0.5 µA × CR × BIASC PDRNG = 01 (see above); $I_{BIAS-VCSEL}$ = 2.5 µA × CR × BIASC PDRNG = 1X (see above); $I_{BIAS-VCSEL}$ = 5 µA × CR × BIASC **Open loop:** $I_{BIAS-VCSEL}$ = 86 µA × BIASC
BIASC6	Bias current bit 6	
BIASC5	Bias current bit 5	
BIASC4	Bias current bit 4	
BIASC3	Bias current bit 3	
BIASC2	Bias current bit 2	
BIASC1	Bias current bit 1	
BIASC0	Bias current bit 0 (LSB)	
EQADJ7	Equalizer adjustment bit 7 (MSB)	**Equalizer adjustment setting** EQENA = 0 (see above) Equalizer is turned off and bypassed
EQADJ6	Equalizer adjustment bit 6	
EQADJ5	Equalizer adjustment bit 5	
EQADJ4	Equalizer adjustment bit 4	
EQADJ3	Equalizer adjustment bit 3	

Table 16. Register Functionality (continued)

SYMBOL	REGISTER	FUNCTION
EQADJ2	Equalizer adjustment bit 2	EQENA = 1 (see above)
EQADJ1	Equalizer adjustment bit 1	Maximum equalization for 00000000
EQADJ0	Equalizer adjustment bit 0 (LSB)	Minimum equalization for 11111111
CPSGN	Eye crossing sign bit 7	**Eye cross-point adjustment setting**
CPADJ6	Eye crossing adjustment bit 6 (MSB)	CPSGN = 1 (positive shift)
CPADJ5	Eye crossing adjustment bit 5	Maximum shift for 1111111
CPADJ4	Eye crossing adjustment bit 4	Minimum shift for 0000000
CPADJ3	Eye crossing adjustment bit 3	CPSGN = 0 (negative shift)
CPADJ2	Eye crossing adjustment bit 2	Maximum shift for 1111111
CPADJ1	Eye crossing adjustment bit 1	Minimum shift for 0000000
CPADJ0	Eye crossing adjustment bit 0 (LSB)	
OSW3	Overshoot width adjustment bit 3 (MSB)	**Overshoot width adjustment setting**
OSW2	Overshoot width adjustment bit 2	Maximum width for 1111
OSW1	Overshoot width adjustment bit 1	Minimum width for 0000
OSW0	Overshoot width adjustment bit 0 (LSB)	
OSH3	Overshoot height adjustment bit 3 (MSB)	**Overshoot height adjustment setting**
OSH2	Overshoot height adjustment bit 2	Maximum height for 1111
OSH1	Overshoot height adjustment bit 1	Minimum height for 0000
OSH0	Overshoot height adjustment bit 0 (LSB)	
USW3	Undershoot width adjustment bit 3 (MSB)	**Undershoot width adjustment setting**
USW2	Undershoot width adjustment bit 2	Maximum width for 1111
USW1	Undershoot width adjustment bit 1	Minimum width for 0000
USW0	Undershoot width adjustment bit 0 (LSB)	
USH3	Undershoot height adjustment bit 3 (MSB)	**Undershoot height adjustment setting**
USH2	Undershoot height adjustment bit 2	Maximum height for 1111
USH1	Undershoot height adjustment bit 1	Minimum height for 0000
USH0	Undershoot height adjustment bit 0 (LSB)	
POL	Output polarity switch bit 4	**Output polarity switch bit** 1: pin 18 = MOD+ and pin 19 = MOD- 0: pin 18 = MOD- and pin 19 = MOD+
OCSRC	Offset cancellation source bit 3	**Offset cancellation source bit** 1: loop connected to the output of the output driver. This requires AC coupling of the output. 0: loop connected to the input of the output driver of the main signal path.
OCDIS	Offset cancellation disable bit 2	**Offset cancellation disable bit** 1 = DC offset cancellation is disabled and cross point adjust is enabled 0 = DC offset cancellation is enabled and cross point adjust is disabled
TSDIS	Temperature sensor disable bit 1	**TS disable bit** 1 = temperature sensor disabled 0 = temperature sensor enabled
SPDIS	Signal path disable bit 0	**Signal path disable bit** 1 = main signal path is disabled, wave shaping path is enabled 0 = main signal path is enabled, wave shaping path is enabled
TSHSGN	Temperature sensor shift sign bit 4	**Temperature sensor shift adjustment setting**
TSSH3	Temperature sensor shift bit 3	TSHSGN = 1 for a positive shift
TSSH2	Temperature sensor shift bit 2	TSHSGN = 0 for a negative shift
TSSH1	Temperature sensor shift bit 1	Maximum shift for 1111
TSSH0	Temperature sensor shift bit 0	Minimum shift for 0000
TSLSGN	Temperature sensor slope sign bit 4	**Temperature sensor slope adjustment setting**
TSSL3	Temperature sensor shift bit 3	TSLSGN = 1 for a positive shift

Table 16. Register Functionality (continued)

SYMBOL	REGISTER	FUNCTION
TSSL2	Temperature sensor shift bit 2	TSLSGN = 0 for a negative shift
TSSL1	Temperature sensor shift bit 1	Maximum shift for 1111
TSSL0	Temperature sensor shift bit 0	Minimum shift for 0000
CPRNG1 CPRNG0	Cross point range bit 1 Cross point range bit 0	**Cross point adjustment range bits:** Minimum adjustment range for 00 Maximum adjustment range for 11
MODRNG1 MODRNG0	Modulation current reduction bit 1 Modulation current reduction bit 0	**Modulation current range reduction bits:** 00 = no reduction in modulation current and step size 01 = current range and step size reduced by a factor of 0.833 10 = current range and step size reduced by a factor of 0.66 11 = current range and step size reduced by a factor of 0.5

LASER SAFETY FEATURES AND FAULT RECOVERY PROCEDURE

The ONET8501V provides built in laser safety features. The following fault conditions are detected:

1. Voltage at MONB exceeds the voltage at RZTC (1.16V),
2. Photodiode current exceeds 150% of its set value,
3. Bias control DAC drops in value by more than 50% in one step

If one or more fault conditions occur and the fault enable bit FLTEN is set to 1, the ONET8501V responds by:

1. Setting the VCSEL bias current to zero.
2. Setting the modulation current to zero.
3. Setting the peaking current to zero
4. Asserting and latching the FLT pin.

Fault recovery is performed by the following procedure:

1. The disable pin DIS and/or the internal enable control bit ENA are toggled for at least the fault latch reset time t_{RESET}.
2. The FLT pin de-asserts while the disable pin DIS is asserted or the enable bit ENA is de-asserted.
3. If the fault condition is no longer present, the part will return to normal operation with its prior output settings after the disable negate time t_{ON}.
4. If the fault condition is still present, FLT re-asserts once DIS is set to a low level and the part will not return to normal operation.

TYPICAL OPERATION CHARACTERISTICS

Typical operating condition is at V_{CC} = 3.3V, T_A = 25°C, I_{BIASC} = 6 mA, I_{MODC} = 12 mA, V_{IN} = 600 mVpp and no waveform shaping (unless otherwise noted).

DETERMINISTIC JITTER
vs
MODULATION CURRENT

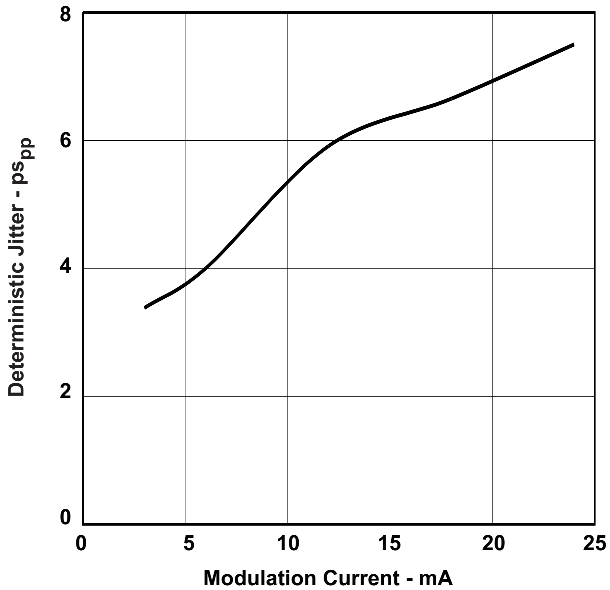


Figure 4.

DETERMINISTIC JITTER
vs
TEMPERATURE

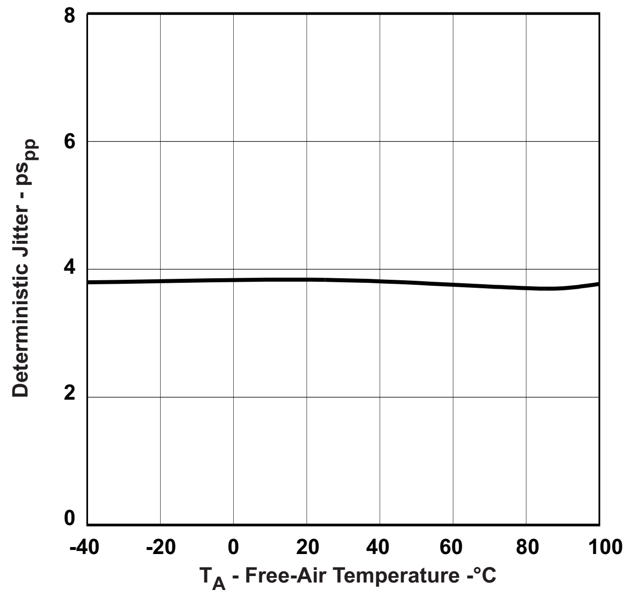


Figure 5.

RANDOM JITTER
vs
MODULATION CURRENT

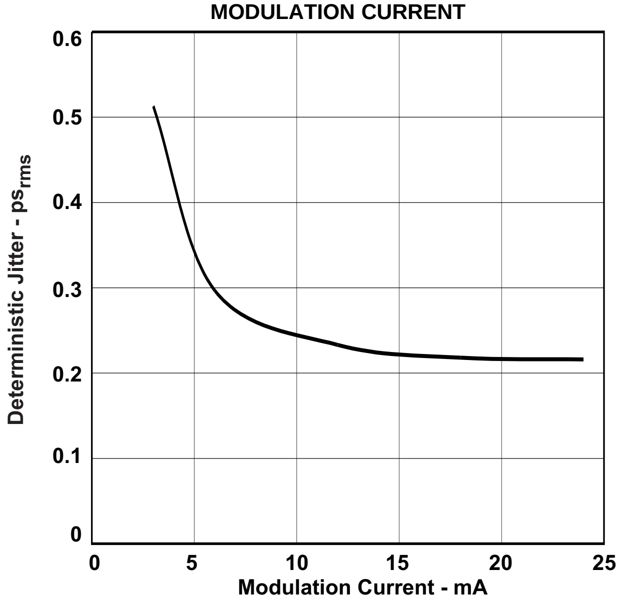


Figure 6.

RANDOM JITTER
vs
TEMPERATURE

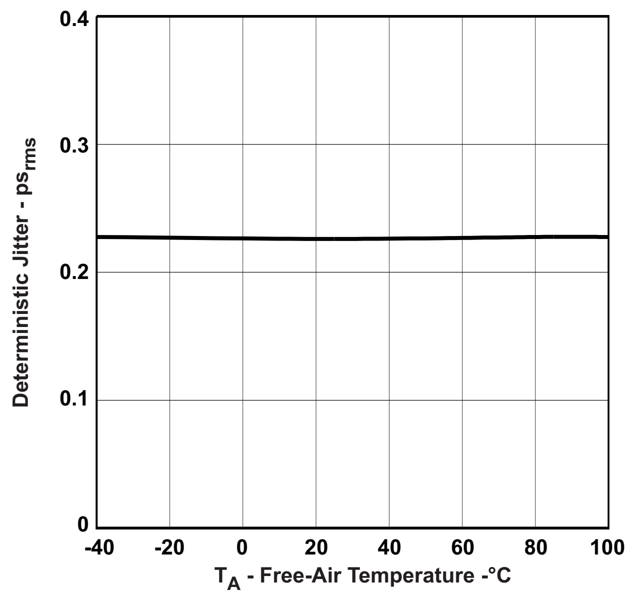


Figure 7.

TYPICAL OPERATION CHARACTERISTICS (continued)

Typical operating condition is at V_{CC} = 3.3V, T_A = 25°C, I_{BIASC} = 6 mA, I_{MODC} = 12 mA, V_{IN} = 600 mVpp and no waveform shaping (unless otherwise noted).

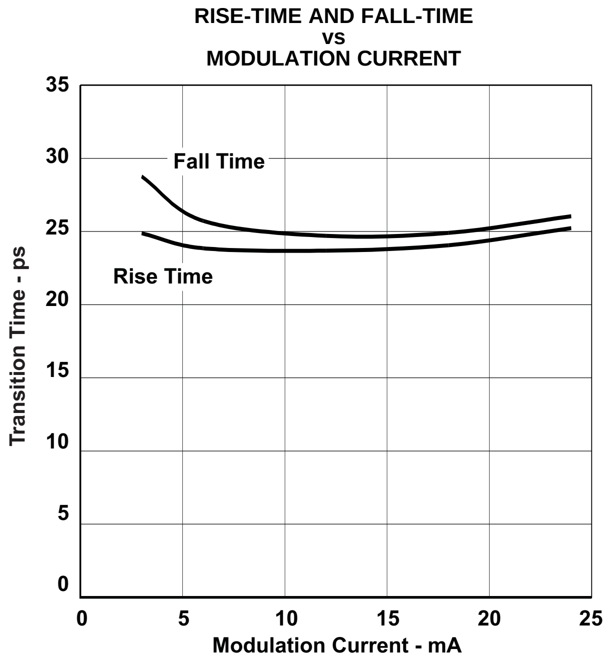


Figure 8.

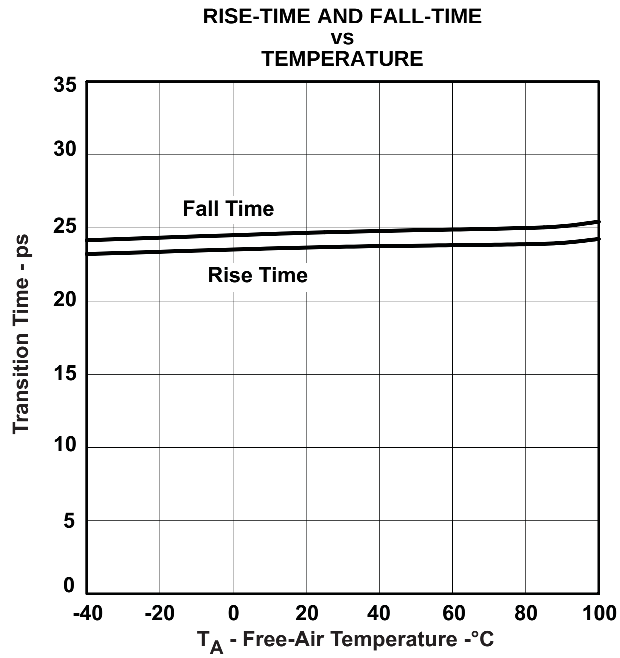


Figure 9.

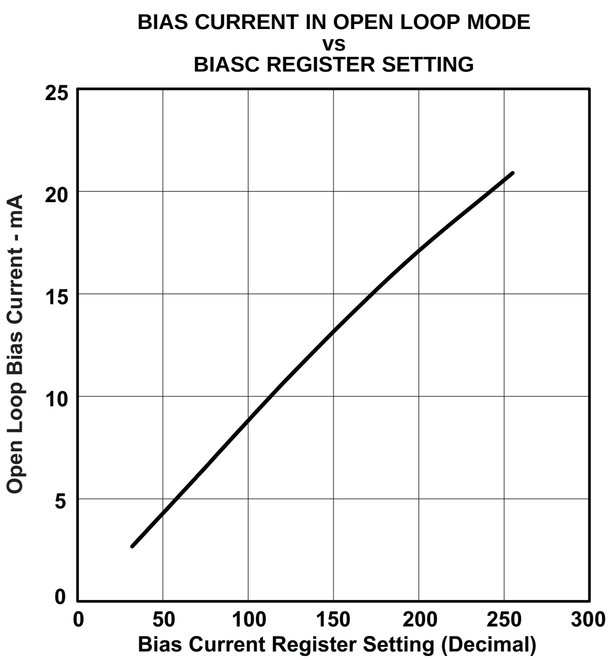


Figure 10.

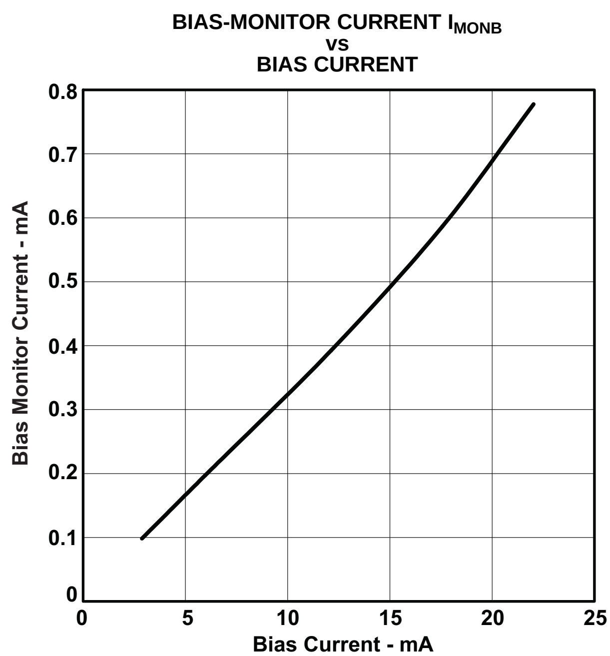


Figure 11.

TYPICAL OPERATION CHARACTERISTICS (continued)

Typical operating condition is at V_{CC} = 3.3V, T_A = 25°C, I_{BIASC} = 6 mA, I_{MODC} = 12 mA, V_{IN} = 600 mVpp and no waveform shaping (unless otherwise noted).

PHOTODIODE-MONITOR CURRENT I_{MONP} vs PD CURRENT, PDR = 00

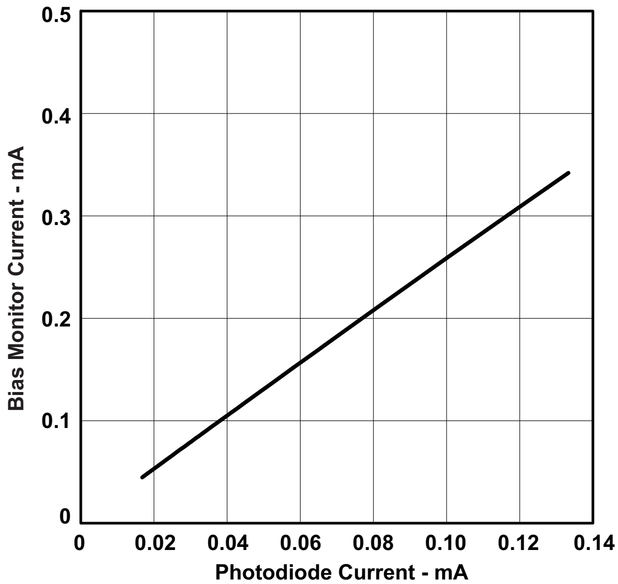


Figure 12.

MODULATION CURRENT vs MODC REGISTER SETTING

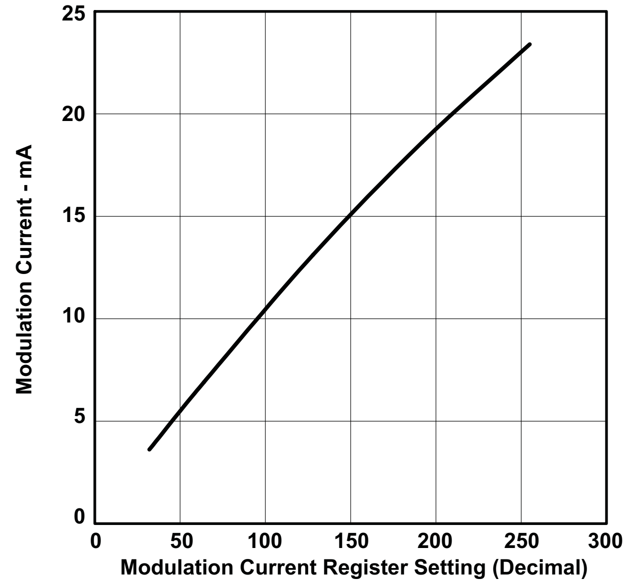


Figure 13.

SUPPLY CURRENT vs TEMPERATURE

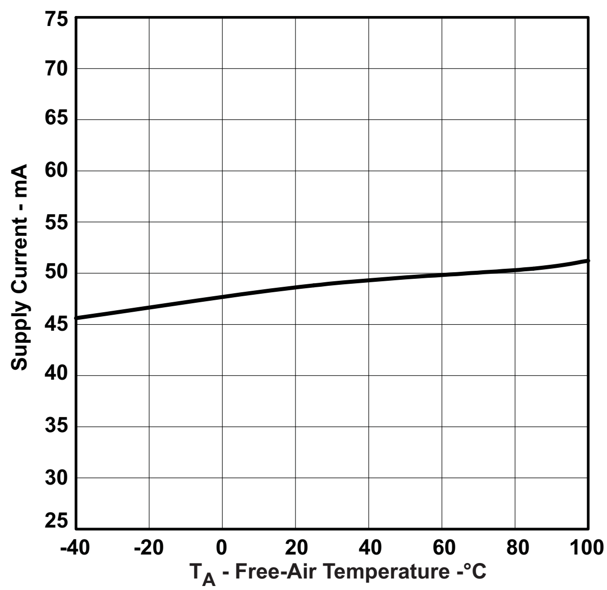


Figure 14.

TEMPERATURE SENSOR VOLTAGE V_{TS} vs TEMPERATURE

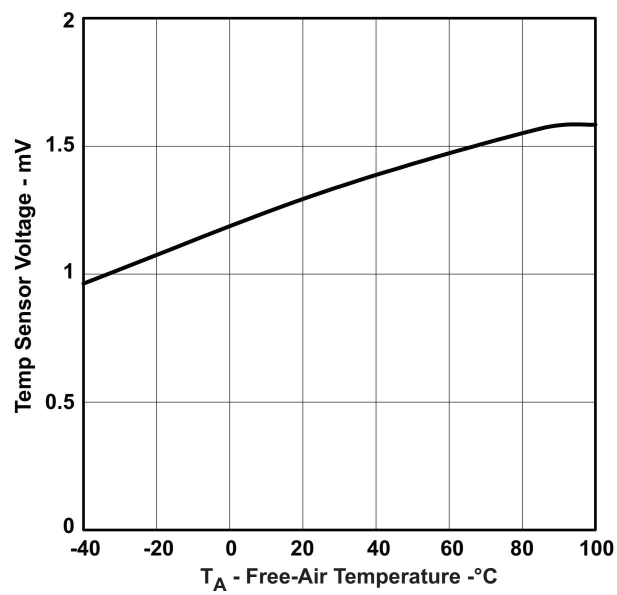


Figure 15.

TYPICAL OPERATION CHARACTERISTICS (continued)

Typical operating condition is at V_{CC} = 3.3V, T_A = 25°C, I_{BIASC} = 6 mA, I_{MODC} = 12 mA, V_{IN} = 600 mVpp and no waveform shaping (unless otherwise noted).

EYE-DIAGRAM AT 11.3GBPS
K28.5 PATTERN, I_{MOD}=6mA, EQENA = 0

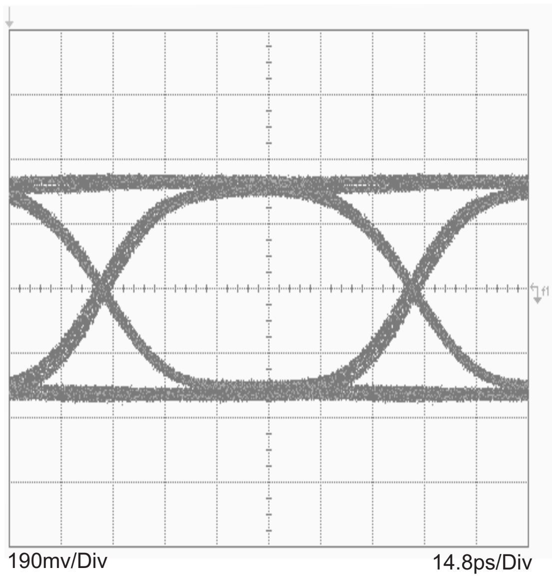


Figure 16.

EYE-DIAGRAM AT 11.3GBPS
K28.5 PATTERN, I_{MOD}=10mA, EQENA = 0

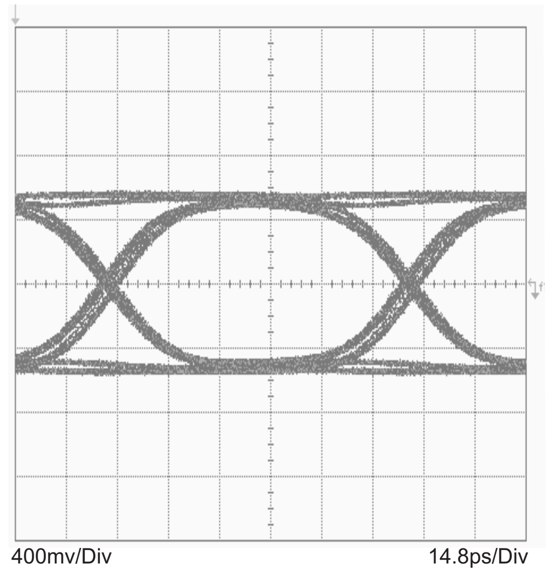


Figure 17.

EYE-DIAGRAM AT 11.3GBPS
K28.5 PATTERN, I_{MOD}=6mA, EQENA = 0,
OSH = USH = 8, OSW = USW = 2, PKRNG = 0

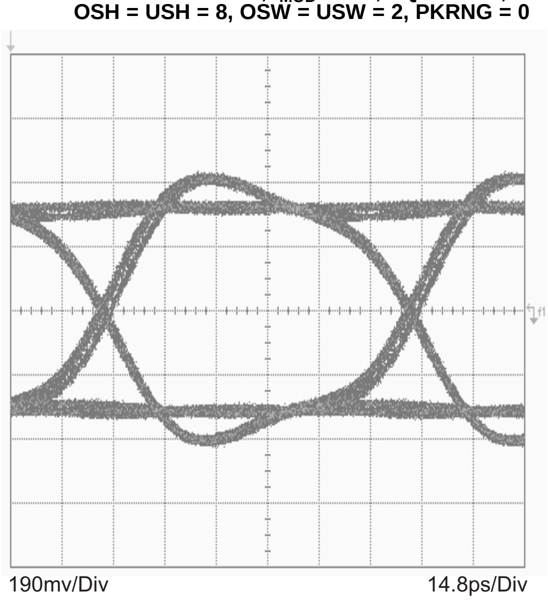


Figure 18.

EYE-DIAGRAM AT 8.5GBPS
K28.5 PATTERN, I_{MOD}=6mA, EQENA = 0

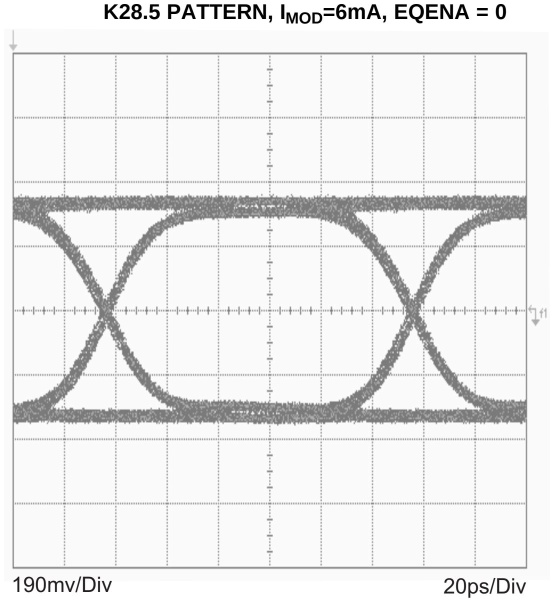


Figure 19.

TYPICAL OPERATION CHARACTERISTICS (continued)

Typical operating condition is at V_{CC} = 3.3V, T_A = 25°C, I_{BIASC} = 6 mA, I_{MODC} = 12 mA, V_{IN} = 600 mVpp and no waveform shaping (unless otherwise noted).

EYE-DIAGRAM AT 11.3GBPS
K28.5 PATTERN, I_{MOD}=6mA,
EQENA = 1, 12" OF FR4 AT INPUTS

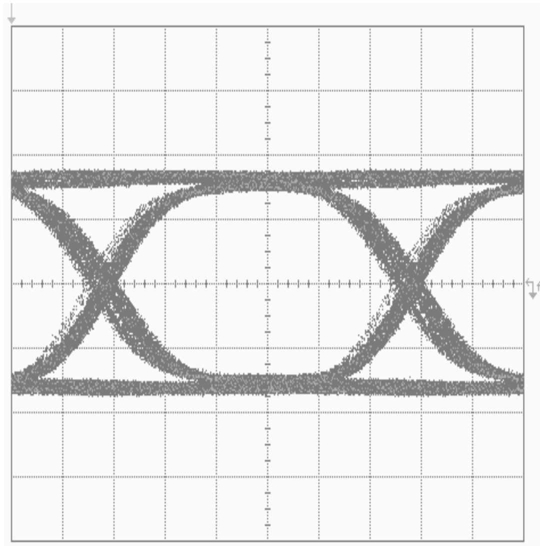


Figure 20.

APPLICATION INFORMATION

Figure 21 shows a typical application circuit using the ONET8501V with a VCSEL diode, anode connected to VCC, and driven differentially. The VCSEL driver is controlled via the 2-wire interface SDA/SCK by a microcontroller. In a typical application, the FLT, MONP, MONP and TS outputs are also connected to the microcontroller for transceiver management purposes.

The component values in Figure 21 are typical examples and may be varied according to the intended application. Single-ended VCSEL drive can be done by terminating the unused driver output in a resistance that matches the VCSEL series resistance, however, the available VCSEL modulation current will be halved.

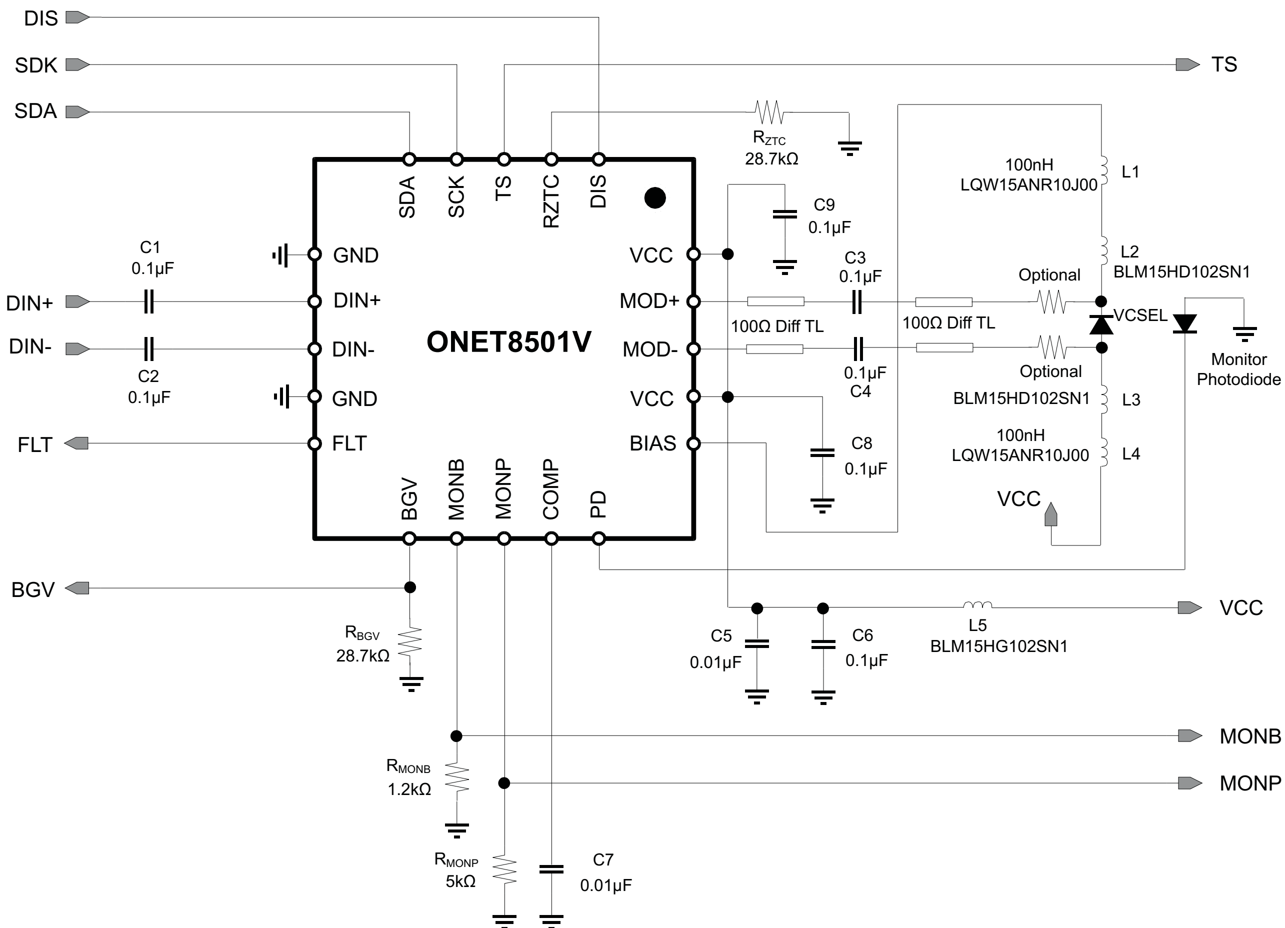


Figure 21. Typical Application Circuit With a Differential Driven VCSEL

In the recommended application circuit, the purpose of the optional series resistors is to improve the signal integrity between the VCSEL driver and the VCSEL. Since the VCSEL impedance varies depending on its type, the series resistor may provide better matching impedance for the modulation current outputs.

LAYOUT GUIDELINES

For optimum performance, use 50Ω transmission lines (100Ω differential) for connecting the signal source to the DIN+ and DIN– pins and for connecting the modulation current outputs, MOD+ and MOD–, to the VCSEL. The length of the transmission lines should be kept as short as possible to reduce loss and pattern-dependent jitter. It is recommended to assemble the series matching resistors as close as possible to the TOSA.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
ONET8501VRGPR	ACTIVE	QFN	RGP	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ONET8501VRGPRG4	ACTIVE	QFN	RGP	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ONET8501VRGPT	ACTIVE	QFN	RGP	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ONET8501VRGPTG4	ACTIVE	QFN	RGP	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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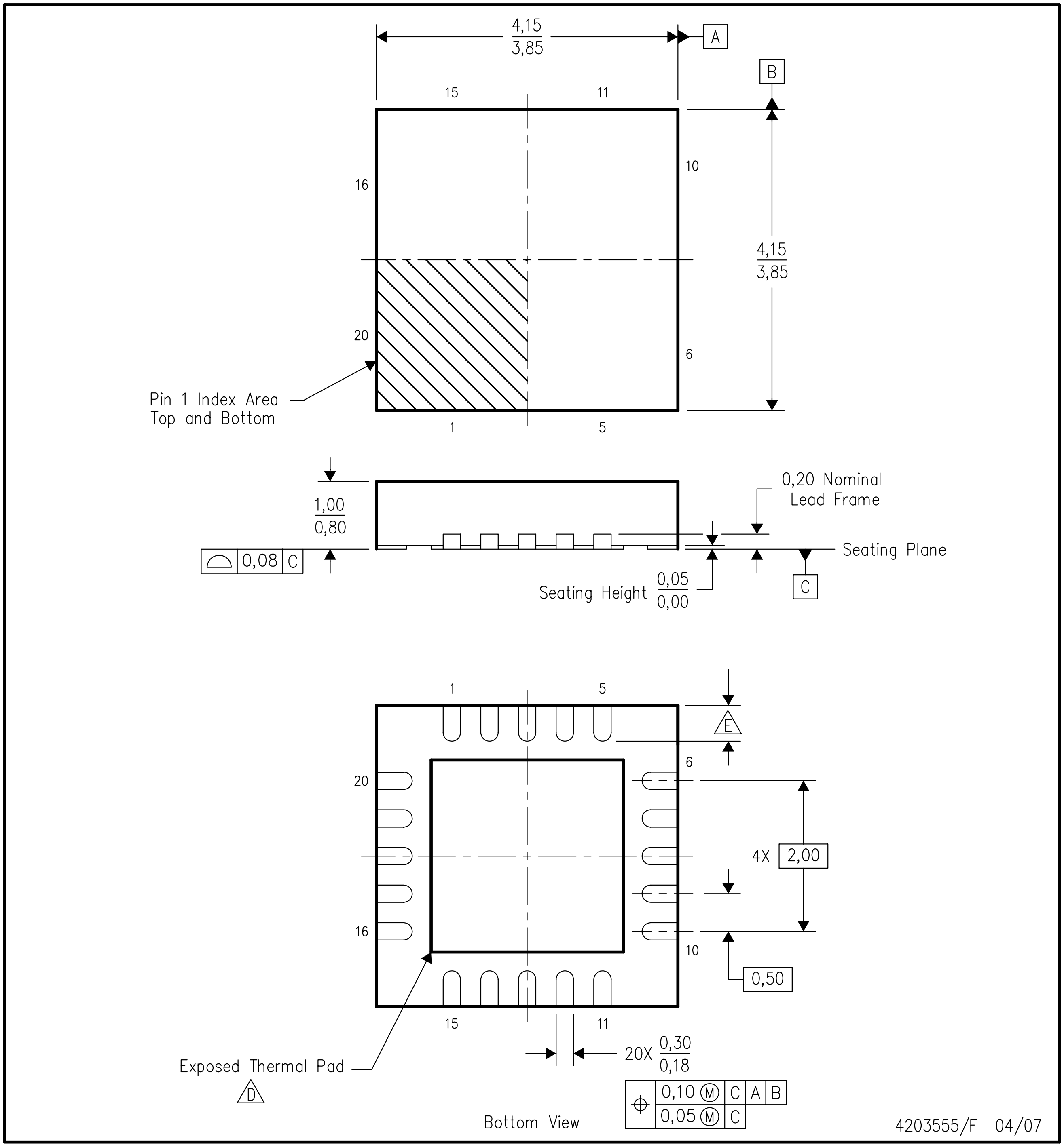
RGP (S–PQFP–N20) PLASTIC QUAD FLATPACK



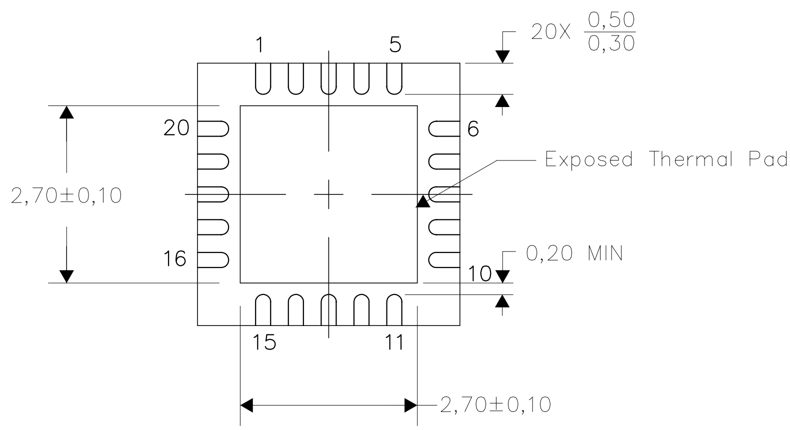
NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No–Lead) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
- E. Check thermal pad mechanical drawing in the product datasheet for nominal lead length dimensions.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

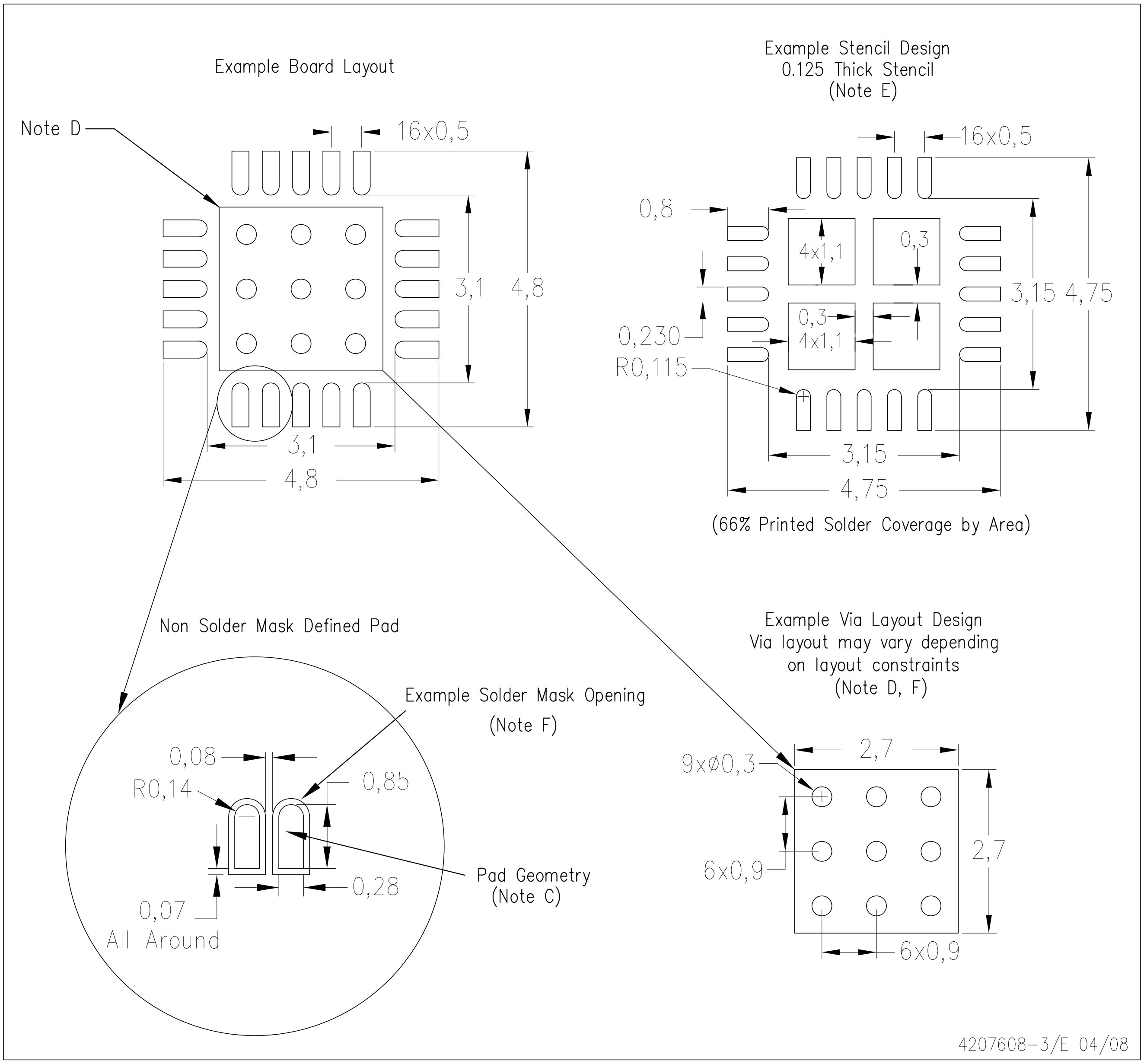


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

RGP (S-PVQFN-N20)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.